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BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Junichi KOKUDO
HIGH SPEED TIMESLOT ASSIGNMENT UNIT
AND METHOD FOR A TDMA
COMMUNICATION SYSTEM
Our Ref. Q61990

Dear Sir:

09721959 - 112700

Attached hereto is the application identified above including 12 sheets of the specification, claims, 3 sheets of informal drawings, and a copy of the executed Declaration and Power of Attorney. The Assignment will be filed at a later date.

The Government filing fee is calculated as follows:

Total claims	6 - 20	=		x	$18.00	= $.00
Independent claims	3 - 3	=		x	$80.00	= $.00
Base Fee						$710.00
TOTAL FEE						**$710.00**

A check for the statutory filing fee of $710.00 is attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. § 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from November 26, 1999 based on Japanese Application No. 11-336763. The priority document will be filed at a later date.

Respectfully submitted,
SUGHRUE, MION, ZINN,
MACPEAK & SEAS, PLLC
Attorneys for Applicant

By: _____
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TITLE OF THE INVENTION

High Speed Timeslot Assignment Unit and Method for a TDMA Communication System

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to TDMA or TDMA/TDD (time division multiple access/time division duplex) wireless communication systems, and more specifically to a timeslot assignment system and method for a TDMA or TDMA/TDD wireless communication system.

Description of the Related Art

Fig. 1 illustrates a prior art timeslot assignment unit of a TDMA/TDD cell-site station of a mobile communication network. The prior art timeslot assignment unit includes a reception unit 10, a slot status memory 11, a control data generation/sequence control (CDG/SC) unit 12 and an assignment table 13. Reception unit 10 is arranged to receive information indicating requirements, or assignment terms to be met for each timeslot to be assigned. In response to an assignment request signal, the reception unit 10 accesses the status memory 11 to check to see if the timeslots requested can be accommodated or not, and sends back a response to the requesting source with an indication as to the check result. If all the requested timeslots can be accommodated, the reception unit 10 sends an assignment command signal to the CDG/SC unit 12. In response to the assignment command signal, the CDG/SC unit 12 receives the assignment terms and produces therefrom a plurality of control data and stores them into the assignment table 13, the contents of which are used by a framing unit when a frame is formulated for

transmission. The control data stored in the assignment table 13 must be reordered in such a sequence that it conforms to the sequence in which frames are transmitted. However, the reordering is based on the memory swapping principle, and hence it requires a complex logic circuit. Because of the complex logic circuitry, the prior art timeslot assignment unit cannot operate at a high speed.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a high speed timeslot assignment unit and method for TDMA or TDMA/TDD communication systems.

The high speed operation is attained by using pointer addressing instead of prior art memory swapping.

According to a first aspect, the present invention provides a slot assignment unit for use in a TDMA transmitter, which comprises first and second tables. A control data generation unit is provided for receiving assignment terms for a plurality of time slots and slot data from an external source, producing a set of assignment control data according to the assignment terms and the slot data and storing the set of assignment control data into an entry of the first table in response to a command signal applied thereto. A sequence controller analyzes a plurality of sets of assignment control data, produces a plurality of address pointers, and stores address pointers in the second table in such a sequence that the address pointers can be sequentially read out in a desired transmission sequence, and supplies the command signal to the control data generation unit in response to each of the address pointers.

According to a second aspect, the present invention provides a TDMA transmitter comprising a first table, a second table, a control data generation unit for receiving assignment terms for a plurality of time slots and slot data from an external source, producing a set of assignment control data according to the assignment terms and the slot data and storing the set of assignment control data into an entry of the first table in response to a command signal applied thereto. A sequence controller is provided for analyzing a plurality of sets of assignment control data, producing a plurality of address pointers, storing the address pointers in the second table in such a sequence that the address pointers can be sequentially read out from a starting address, and supplying the command signal to the control data generation unit in response to each of the address pointers. A framing unit sequentially reads address pointers from the starting address of the second table and reads assignment control data from entries of the first table specified by the read address pointers and formulates a frame with the read assignment control data.

According to a third aspect, the present invention provides a slot assignment method for a TDMA transmitter, comprising the steps of (a) receiving assignment terms for a plurality of time slots, (b) producing a set of assignment control data according to the assignment terms, (c) repeating steps (a) and (b) to produce a plurality of sets of assignment control data, (d) analyzing said plurality of sets of assignment control data, (e) storing one of said sets of assignment control data into an entry of a first table, (f) storing an address pointer in a second table corresponding to said entry of said first table, and (g) repeating steps (d) to (f) until all assignment control data are stored in the first table. The slot assignment method may further includes the

steps of sequentially reading address pointers from a starting address of the second table and reading assignment control data from the first table in accordance with the read address pointers, and formulating a frame with the read assignment control data.

BRIEF DESCRIPTION OF THE DRAWIGNS

The present invention will be described in detail further with reference to the following drawings, in which:

Fig. 1 is a block diagram of a prior art slot assignment unit of a TDMA/TDD cell-site station;

Fig. 2 is a block diagram of a TDMA/TDD cell-site system in which the timeslot assignment unit of the present invention is incorporated;

Fig. 3 is a block diagram of the slot assignment unit of the present invention; and

Fig. 4 is a flowchart of the operation of a sequence controller according to the present invention.

DETAILED DESCRIPTION

Referring now to Fig. 2, there is shown a transceiver that can be used in a demand-assigned dynamic TDMA (time division multiple access) system or a dynamic TDMA/TDD (time division multiple access/time division duplex) system in which a TDMA frame is segmented into timeslots (or simply slots) and transmit/receive unit data, or packets (such as data packets and control packets) are assigned to a plurality of slots and scheduled on an on-demand basis. The transceiver is particularly designed to be used as a cell-site station of a TDMA cellular mobile communication network.

The TDMA/TDD scheduling and framing functions of a cell-site

station is embodied in the transceiver of Fig. 2, in which the cell-site station is comprised of a slot assignment unit 21, a TDMA/TDD framing unit 22 to which a modem 29 is connected, a memory controller 13 with which a data memory 24 is associated, a CPU 25, a ROM 26 and a RAM 27, all of which are connected to a common bus 28. CPU 25 operates according to a programmed routine stored in the ROM 16 to perform memory control, TDMA/TDD scheduling, framing and slot assignment control. RAM 27 serves as a work area for data to be processed by the CPU 25. Data memory 24 is accessed by the memory controller 23 to store data to be transmitted to or received from mobile terminals via the framing unit 22.

CPU 25 constantly monitors the contents of the data memory 24 via the memory controller. When a data packet or a control packet is stored in the data memory 24, the CPU 25 determines the size of the packet, the address of the packet in the data memory 24, the packet type, and the destination address and produces an assignment request signal containing these items of slot data. CPU 25 further produces information regarding the requirements or assignment terms to be met for each time slot to be assigned. The assignment terms information include priority levels classified according to communication services and urgency, type of packets, and uplink-to-downlink ratio within the frame.

As shown in detail in Fig. 3, the slot assignment unit 21 is comprised of a reception unit 30, a status memory 31, a control data generation (CDG) unit 32, a control data table 33, a sequence controller 34 and an address pointer table 35.

From the CPU 25, the reception unit 30 receives the assignment

request signal and the assignment terms signal. In response to the assignment request signal, the reception unit 30 calculates the number of slots that can be assigned to TDMA frames based on data contained in the request signal as well as on the assignment terms and accesses the status memory 31 to check to see if the determined slots can be accommodated or not by the currently available slots, and sends back a response to the CPU 25 indicating the result of the check.

If all the requested slots can be accommodated, the reception unit 30 sends an assignment command signal to the CDG unit 32. In response to the command signal, the CDG unit 32 receives the assignment request signal and the assignment terms signal from the reception unit 30. By using the assignment terms, the CDG unit 32 produces a set of assignment control data for the assignment unit (ten slots, for example) and produces a plurality of sets of assignment control data by repeatedly receiving assignment request signals. CDG unit 32 holds the sets of assignment control data until it receives a transfer command signal from the sequence controller 34 for each entry of the control data table 33.

Each set of assignment control data includes data type, mobile address, communication mode, starting address of slots in the data memory 24, the number of slots contained in an assignment unit, the address of the assigned slot in the data memory 24 and ancillary data. When each set of assignment control data is produced, the CDG unit 32 updates the slot status memory 31. When the slot status memory 31 is overflowed, assignment request from the CPU 25 will be rejected. For each assignment request from the CPU 25, a set of assignment control data is stored in one entry of the

control data memory 33.

Sequence controller 34 responds to the start timing signal from the framing unit 22 by analyzing a plurality of sets of assignment control data maintained in the CDG unit 32 and sequentially produces address pointers according to the TDMA slot assignment rule, indicating the addresses of the entries of the control data table 33. The address pointers are stored into an address pointer table 35 such that corresponding assignment control data are read out from the control data table 33 in the same sequence as time slots are transmitted from the cell-site station. Address pointer table 35 may be implemented in a configuration similar to a shift register in which stored address pointers are automatically shifted when a new address pointer is stored if the storage location of the new pointer is ahead of, or in between, the previously stored pointers.

As shown in Fig. 4, the write operation of the sequence controller 34 starts with decision step 41 when the start timing signal is received from the framing unit 22 and analyzes a plurality of sets of assignment control data maintained in the CDG unit 32 (step 42). At step 43, the sequence controller 34 supplies a transfer command signal to the CDG unit 32 to transfer its assignment control data into the first entry of the slot data table 33 and produces a corresponding address pointer and stores it in the first entry of the address pointer table 35 (step 44). If all assignment control data of the current assignment unit have been stored (step 45), the sequence controller 34 terminates the routine. If not, the sequence controller 34 returns to step 42 to repeat the same process until all assignment control data of the assignment unit are stored in the control data table 33 with their corresponding address

pointers in the address table 35. Therefore, steps 42 to 45 are repeatedly performed a number of times corresponding in number to assignment request signals received from the CPU 25.

When a frame is formulated, the framing unit 22 sequentially reads address pointers from the starting address of the address pointer table 35. Using the read address pointers, the framing unit reads the contents of the control data table 32 and inserts transmit data into assigned slots of the frame for transmission.

What is claimed is:

1. A slot assignment unit for use in a time division multiple access (TDMA) transmitter, comprising:

a first table;

a second table;

a control data generation unit for receiving assignment terms for a plurality of time slots and slot data from an external source, producing a set of assignment control data according to the assignment terms and the slot data and storing the set of assignment control data into an entry of said first table in response to a command signal applied thereto; and

a sequence controller for analyzing a plurality of said sets of assignment control data, producing a plurality of address pointers, storing said plurality of address pointers in said second table in such a sequence that the address pointers can be sequentially read out in a desired transmission sequence, and supplying said command signal to said control data generation unit in response to each of said address pointers.

2. The slot assignment unit of claim 1, wherein said TDMA transmitter includes a data memory for storing a plurality of transmit data, and wherein said set of assignment control data stored in said first table includes an address of a communication terminal, a starting address point of each transmit data in said data memory, and a count number of slots assigned to said entry.

3. A time division multiple access (TDMA) transmitter

comprising:

a first table;

a second table;

a control data generation unit for receiving assignment terms for a plurality of time slots and slot data from an external source, producing a set of assignment control data according to the assignment terms and the slot data and storing the set of assignment control data into an entry of said first table in response to a command signal applied thereto; and

a sequence controller for analyzing a plurality of said sets of assignment control data, producing a plurality of address pointers, storing said plurality of address pointers in said second table in such a sequence that the address pointers can be sequentially read out from a starting address of the second table, and supplying said command signal to said control data generation unit in response to each of said address pointers;

a data memory for storing a plurality of transmit data; and

a framing unit for sequentially reading address pointers from said starting address of said second table and reading assignment control data from entries of said first table which are specified by the read address pointers and formulating a frame with the read assignment control data and said plurality of transmit data from said data memory.

4. The TDMA transmitter of claim 3, wherein said set of assignment control data stored in said first table includes an address of an assigned communication terminal, a starting address point of each transmit data in said data memory, and a count number of assigned slots.

5. A slot assignment method for a time division multiple access (TDMA) transmitter, comprising the steps of:

a) receiving assignment terms for a plurality of time slots and slot data;

b) producing a set of assignment control data according to the assignment terms and the slot data;

c) repeating steps (a) and (b) to produce a plurality of sets of assignment control data;

d) analyzing said plurality of sets of assignment control data;

e) storing one of said sets of assignment control data into an entry of a first table;

f) storing an address pointer in a second table corresponding to said entry of said first table; and

g) repeating steps (d) to (f) until all of said assignment control data are stored in the first table.

6. The slot assignment method of claim 5, further comprising the steps of:

sequentially reading address pointers from a starting address of said second table and reading said plurality of sets of assignment control data from said first table in accordance with the read address pointers; and

formulating a frame with the assignment control data read from the first table.

ABSTRACT OF THE DISCLOSURE

In a TDMA/TDD transmitter, a control data generation unit receives assignment terms for a number of time slots and slot data from an external source, produces a set of assignment control data according to the assignment terms and the slot data and stores the set of assignment control data into an entry of a control data table in response to a transfer command signal. A sequence controller analyzes sets of assignment control data maintained in the control data generation unit and produces a number of address pointers. The address pointers are stored in an address pointer table in such a sequence that they can be sequentially read out in a desired transmission sequence. The aforesaid transfer command signal is supplied from the sequence controller to the control data generation unit in response to each of the address pointers. A framing unit sequentially reads address pointers from the starting address of the address pointer table, reads assignment control data from the control data table in accordance with the read address pointers, and formulates a frame. Transmit data stored in a data memory is inserted into the frame for transmission.

FIG. 1
PRIOR ART

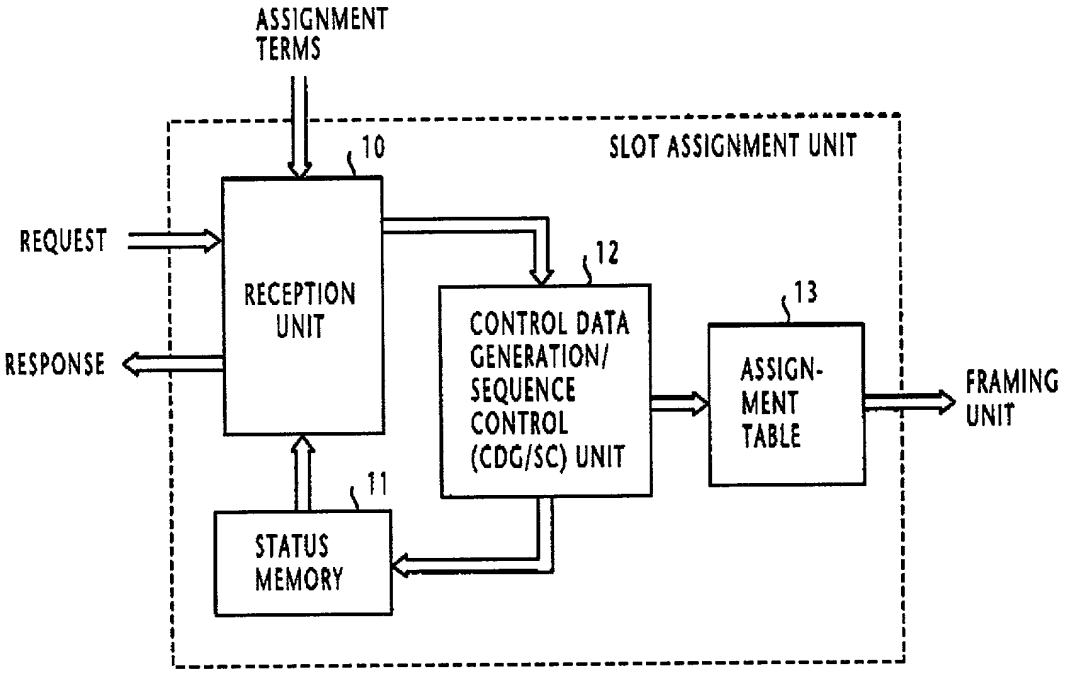


FIG. 2

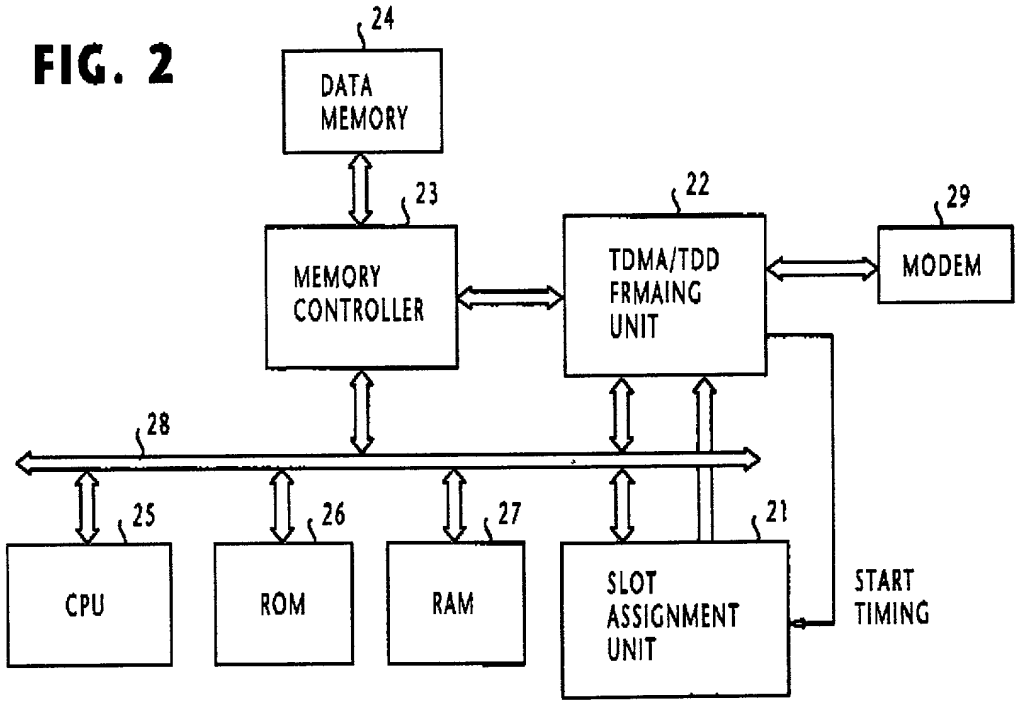


FIG. 3

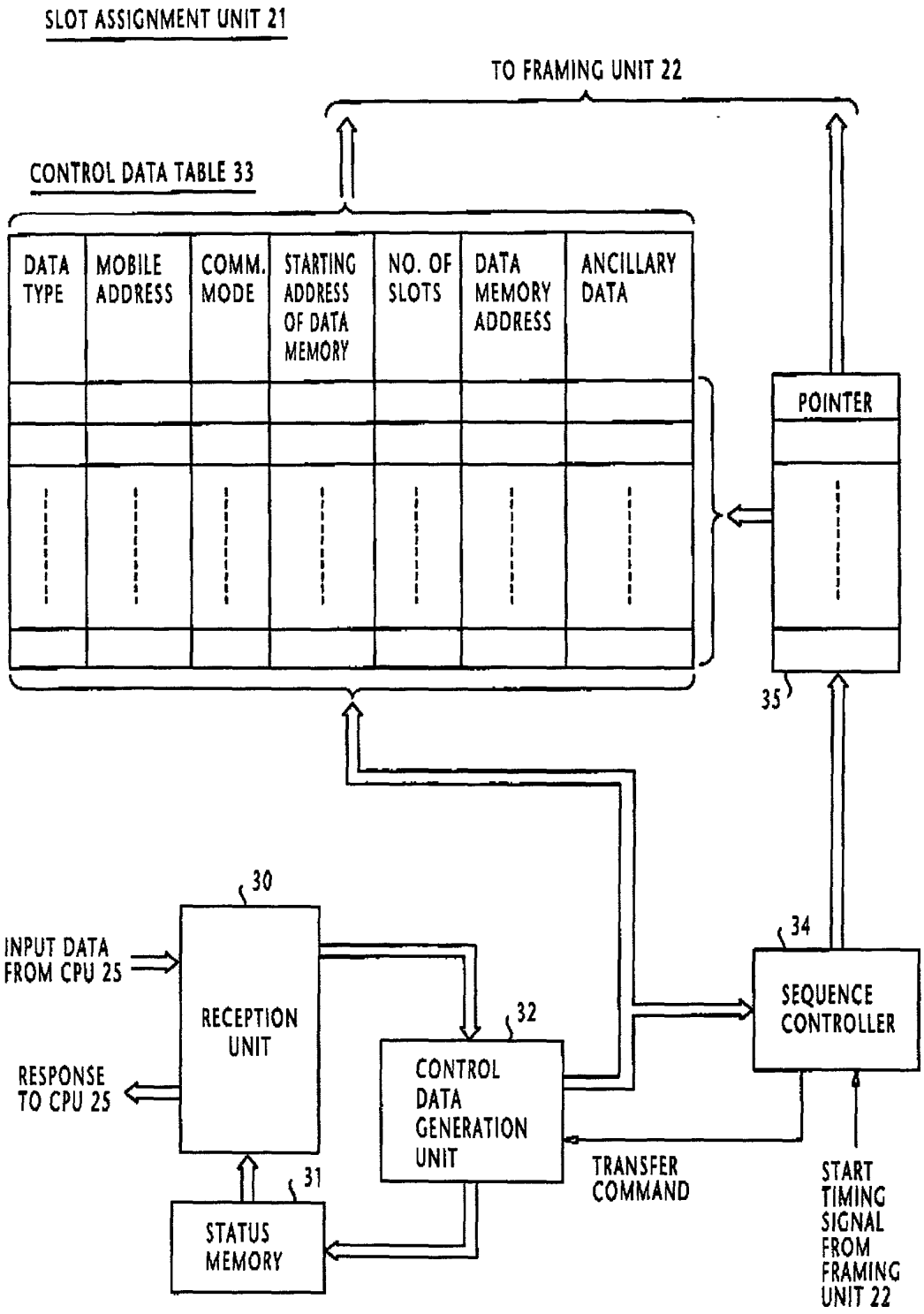
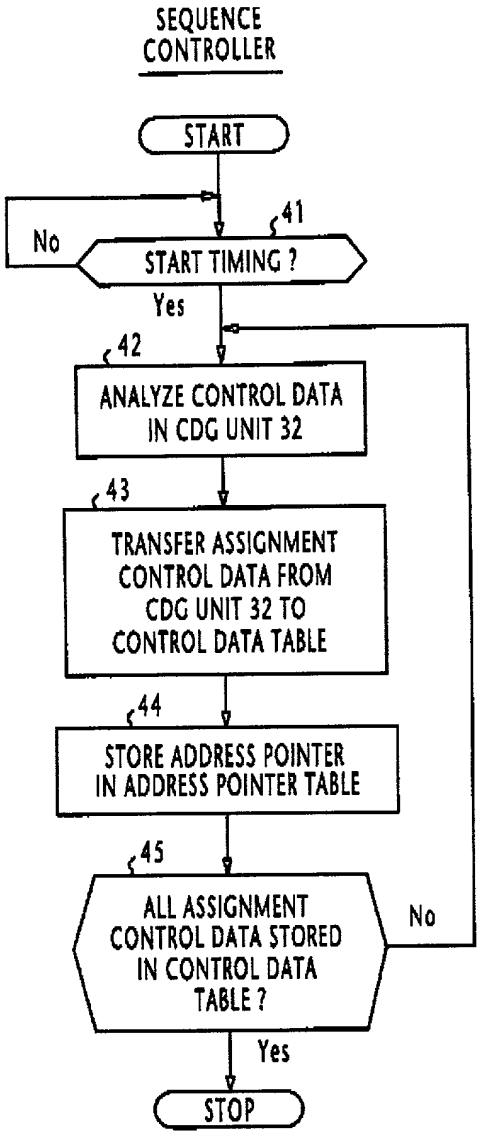

SLOT ASSIGNMENT UNIT 21
TO FRAMING UNIT 22
CONTROL DATA TABLE 33
DATA TYPE
MOBILE ADDRESS
COMM. MODE
STARTING ADDRESS OF DATA MEMORY
NO. OF SLOTS
DATA MEMORY ADDRESS
ANCILLARY DATA
POINTER
35
30
INPUT DATA FROM CPU 25
RECEPTION UNIT
RESPONSE TO CPU 25
32
CONTROL DATA GENERATION UNIT
34
SEQUENCE CONTROLLER
31
STATUS MEMORY
TRANSFER COMMAND
START TIMING SIGNAL FROM FRAMING UNIT 22

FIG. 4


SEQUENCE CONTROLLER
START
41
No
START TIMING ?
Yes
42
ANALYZE CONTROL DATA IN CDG UNIT 32
43
TRANSFER ASSIGNMENT CONTROL DATA FROM CDG UNIT 32 TO CONTROL DATA TABLE
44
STORE ADDRESS POINTER IN ADDRESS POINTER TABLE
45
ALL ASSIGNMENT CONTROL DATA STORED IN CONTROL DATA TABLE ?
No
Yes
STOP

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name: that I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought in the application entitled:

High Speed Timeslot Assignment Unit and Method for a TDMA Communication System .

which application is:

_X_ the attached application (for original application)

___ application Serial No. _____, filed _____, and amended on _____ (for declaration not accompanying application)

that I have reviewed and understand the contents of the specification of the above-identified application, including the claims, as amended by any amendment referred to above; that I acknowledge my duty to disclose information of which I am aware which is material to the patentability of this application under 37 C.F.R. 1.56, that I hereby claim foreign priority benefits under Title 35, United States Code §119, §172 or §365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified on said list any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date	Priority Claimed (yes or no)
11-336763	Japan	November 26, 1999	Yes

I hereby claim the benefit of Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in a listed prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge my duty to disclose any information material to the patentability of this application under 37 C.F.R. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778 and Abraham J. Rosner, Reg. No. 33,276, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to SUGHRUE, MION, ZINN, MACPEAK & SEAS, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date November 22, 2000

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